Corporate Electronics - Packaging and Interconnect Strategy

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ABSTRACT: The Corporate Electronics Packaging and Interconnect Strategy defines the process and technology introduction roadmap for physical technologies extending from the chip edge through the backplane level.

APPLICABILITY: The Corporate Electronics Packaging and Interconnect Strategy provides guidance for and is influenced by the manufacturing process strategy, which is the responsibility of the Module Process Management Committee and the Electronics Technology File, which is the province of the Module Design Committee.

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1 ELECTRONIC PACKAGING WORKING GROUP (EPWG)

The Electronic Packaging Working Group (EPWG) strategy is the technology introduction roadmap for the physical elements to be used for cross-product electronics design.

In constructing the strategy, future product needs are of paramount importance. It is also crucial that the strategy be formed by technical and business judgments and the realization that Digital needs only a limited subset of all available technologies to be embodied in the strategy.

The EPWG strategy provides guidance for, and is influenced by, the manufacturing process strategy, which is the responsibility of the Module Process Management Committee (MPMC) and by the Electronics Technology File, which is the province of the Module Design Committee.

1.1 EPWG STRATEGY ROADMAPS

- **Chart 1:**
  Shows committed developments with anticipated technology requirements shown in italics.

- **Chart 2:**
  Shows exploratory developments sanctioned by the EPWG.

- The technology platform concept is intended to be backward-compatible: products need not be designed to the most advanced technology. The cross-organizational Module Design Committee (MDC) and Module Process Management Committee (MPMC) have the responsibility to retire technologies.
- The platform concept provides a framework for the Electronics Technology File for design and stable process specifications for manufacturing.

CHART 1 - BASE ELECTRONICS TECHNOLOGY ROADMAP-MAINSTREAM TECHNOLOGIES

Mainstream Technologies

Mar–92

Technology	Prototype Year							
	FY89	**FY90**	**FY91**	**FY92**	**FY93**	**FY94**	**FY95**	**FY96**
Semiconductor Technology	**CMOS 3**	**Mosaic 3**	**CMOS 4**		**CMOS5 (EV5)**			*CMOS6 (EV6)*
Chip Termination		**SWB3**	**SWB4**		**SWB5**			*CTI6*
Singlechip Packages		**SCP3**	**SCP4**		**SCP5**			*SCP6*
Multichip Packages		**MCU1**						
Connectors	**Teradyne HD+**			**IEEE 2mm**	**HD+2**			
Printed – wiring Board	**PWB4**					**PWB5**		
Module Technology		**MP3**		**MP4**		**MP5**		*MP6* →
Backplane Assemblies								
	T3 Technology Platform ↔		T4 Technology Platform ↔		T5 Technology Platform ↔			T6 Technology Platform

Boldfaced: committed developments

Italics: anticipated technology requirements

See Glossary for definitions.

- "Prototype year" indicates that
  - Characterization data is available and complete.
  - Manufacturing prototypes and test vehicles are available.
  - Engineering (product) prototypes can be built.
  - Full qualification follows in the next year.
  - Tech Files are released.

CHART 2 - TECHNOLOGY EXPLORATORY DEVELOPMENT ROADMAP-ADVANCED/ALTERNATE TECHNOLOGIES

Advanced / Alternate Technologies **Mar–92**

Technology	Decision Year							
	FY89	FY90	FY91	FY92	FY93	FY94	FY95	FY96
Semiconductor Technology				GaAs				
Chip Termination					Flip Chip CACC			
Single Chip Packages			SMPGA	{SPA} {Interposer}	sub 0.5mm SMT			
Multichip Packages				MM1 {MCM–L,C}				
Connectors					SMT Connectors			
Printed–wiring Board								
Module Technology					sub 0.5mm SMT COB			
Backplanes								
	T3 Technology Platform ←		T4 Technology Platform ←		T5 Technology Platform →			T6 Technology

{ }: Decisions have been made.

- "Decision year" indicates date of exploratory development completion. Development work would follow (Chart 1) if results were favorable and the technology was required.
- Product design choices are the responsibility of the user groups and should be synchronized with Chart 1 dates.

1.2 EPWG CHART 2 DECISIONS

- Surface Mount Pin Grid Array (SMPGA): not needed in the foreseeable future. Development to date is adequate.
- Separable Pad Array (SPA) and Interposers (Q1 FY92): these technologies are not needed at the present time, but show promise. (Technologies are "on the shelf").
- MCM-L, MCM-C (Q3 FY92): further exploratory development in multichip technologies is not needed. See Multichip Technology Strategy.

1.3 BASE ELECTRONICS TECHNOLOGY PLATFORM DESCRIPTION

The following table details base electronics technology platform descriptions.

	T3	T4	T5	T6
Tech File Availability	FY90	FY92	FY94	FY96
CMOS Semiconductors				
CMOS Process	CMOS 3	CMOS 4	CMOS 5	CMOS 6
Chip Termination	SWB	SWB	SWB	tbd
Pads/Pad Pitch (u)	327/150	428/125	578/112	1000/tbd
VLSI Single Chip Packages	**SCP3**	**SCP4**	**SCP5**	**SCP6**
THPGA Pins	339	447	503	1000
Pinfield (mils)	100×100	100×100 100×50	100×100 100×50	100×100 100×50
SMT Packages	LDCC, PQFP, CQUAD	PQFP, CQUAD	PQFP	PQFP
Max SMT Pins	224	232*	tbd	tbd
Min Pin Pitch	25 mils	0.65mm	tbd	tbd
Multichip	**MCU1**			
Substrate	CuPI			
Chip Termination	TAB			
OLB Pitch (mils)	8	n/a	n/a	n/a
No. Chips (max)	9			
Max Total Power (W)	250			
Body Size	< >			
Interconnect	Flex			
PWB	**PWB4**	**PWB4**	**PWB5**	**PWB6**
Preferred Material	FR4	FR4	FR4	tbd
Total Layers	10	10	12	tbd
Max Aspect Ratio	9:1	9:1	9:1	tbd
Min Feature (line/space)	0.005/0.005	0.005/0.005	0.004/0.004	tbd
Module Assembly	**MP3**	**MP4**	**MP5**	**MP6**
Mixed Technology (?)	Y	Y	Y	Y
Side 2 Passives	Y	Y	Y	Y
Side 2 Actives	Available	⟶	⟶	⟶
SMT Process	VP Reflow	Hot Air	Hot Air	tbd
Fine Pitch Process	VP Reflow	Hot Air	tbd	tbd
Connectors				
Industry standard buses	⟵	Preferred Standard connectors		⟶
High Performance	HD+	HD+	HD+2	tbd
Others	Various	⟵ Preferred Parts List ⟶		⟶

*** Use of 0.5 mm PQFPs allowed with restrictions; see SCP4 strategy.**

1.4 EPWG ROSTER

Member	Organization
Colin Becker	Europe
Bob Brownell	Semicondutor Operations (SCO)
Dick Crino	General International Area (GIA)
Les Fox	Manufacturing and Design Technology/Technology Development and Architecture (MDT/TDA)
Jim Grochmal	VAX Systems and Servers
Rob Hannemann (chair)	Manufacturing and Design Technology (MDT)
Steve Hansen	Manufacturing and Design Technology/Technology Development and Architecture/TDA
George Katronge	Printed-wiring Boards
Mike Leis	Storage
Dave Moreno	UNIX Systems and Servers
Duane Napp	VAX Systems and Servers
Dave Newman	Networks and Communications
Shlomo Novotny	Personal Computer Systems and Peripherals
Hank Rauch	Module Process Management Committee
Chuck Thacker	Corporate Research and Architecture

1.5 STRATEGY SCOPE

- All Digital electronics development for internal product use
- Multiple product generations
- Die through backplane interconnect levels
- Advanced development through field deployment

1.6 STRATEGY GOALS AND BENEFITS

- **Major goals:**
  - Provide Digital with technologies consistent with world-class cost and performance competitiveness
  - Significantly reduce development investments and operational spending
- **Benefits for engineering**
  - Lower cost
  - Higher quality
  - Lower risk
  - Improved predictability
  - Improved time-to-profit

- **Benefits for manufacturing**
  - Greater process stability and uniformity
  - Lower investments
  - Capacity flexibility

1.7 STRATEGIC PRINCIPLES - 1

- The Corporation's primary area of leverage and investment in electronics is **semiconductor technology**. Future investment in packaging and interconnect technology (P/I) must be adequate to exploit the semiconductor technology (and no more).
- P/I is a core technology set for Digital. A strong development infrastructure in this area is vital.
- Adequate technology maturity should be achieved in advanced development through *DEC STD 084-0 Process and Technology Phase Review Procedure* before product commitment.
- Product commitment should come before significant investment in production process development starts for a new technology.
- Significantly increased attention needs to be paid to competitive technologies for high volume commodity products.

1.8 STRATEGIC PRINCIPLES - 2

- Design for manufacturability, assembly, and test are strategically important focuses.
- Time-to-market (TTM), time-to-volume (TTV), and time-to-profit (TTP) are crucial parameters for our products and must be emphasized in technology development, product design, and manufacturing.
- P/I technologies and related processes used in Digital products should be world class in quality and should be competitive (in cost, performance, reliability, and so on) at the component, subassembly, and assembly levels.
- All materials and processes must be engineered to be consistent with Digital's health, safety, and environmental policies.

1.9 EPWG STRATEGY THEMES

- Technology platforms (generations) are possible and have been sketched.
- Overall, the rate of technology advancement in this technology area can and should be slower in the 90s than it was in the 80s.
- Strategic focus is technology **use** rather than **technology advancement;** emphasis is on **production technology** rather than product technology. We must aim for world leadership in **production performance**.
- In three areas - Printed-wiring board (PWB), surface mount package technology, and backplane connectors - we intend to be at parity (state-of-the-shelf) rather than industry leadership (state-of-the-art).

- In very large scale integration (VLSI) chip packaging, we must be at the state-of-the-art to support our microprocessor strategy while recognizing the importance of low-cost chip packaging for most ICs.
- **A key requirement for success is the need for engineering and manufacturing discipline.**

2 PRODUCT CONTEXTS

2.1 VAX SYSTEMS AND SERVERS (VSS)/DATA CENTER SYSTEMS AND SERVICES (DCSS) CONTEXT

- Strategy is based upon a platform concept for VAX™ and EVMS Architectures
- Mainframe/Mid-Range Platforms
  - VAX 9000 ™ ... VAX ECL multiprocessor
  - VAX 6000™ ... VAX CMOS multiprocessor
  - Laser ... CMOS VAX and Alpha AXP™ multiprocessor platform
- Physical Implementations
  - VAX 9000 .. multi-chip ECL gate-array/custom modules on large planar modules
  - VAX 6000 ... single chip microprocessor CMOS packages on standard PWB modules in backplanes
  - Laser ... single chip microprocessor CMOS packages on standard PWB modules in backplanes
- Historically 2-3 year product introduction cycles and medium volumes
- Four years between platform generations
- Emphasis on reduced cost and time-to-market

2.2 VAX SYSTEMS AND SERVERS ENTRY SYSTEMS BUSINESS (VSS ESB) / ENTRY LEVEL SYSTEMS (ELS) CONTEXT

- Strategy based upon a platform strategy for VAX and EVMS Architectures
- Desktop/Deskside Platforms
  - Desktop (<$25K Entry Price)
  - Deskside ($25K to $75K Entry Price)
  - Deskside (>$75K Entry Price)
- Physical Implementation
  - Single chip CMOS microprocessor packages on standard mother boards
- Aggressive investigation of technologies for higher performance / lower cost
- Two to three year product introduction cycle with medium/high volume
- Increased emphasis on reduction of costs and time-to-market
- Investigation of laptop/notebook/portable form factor products

- Three years between platform generations

2.3 VAX SYSTEMS AND SERVERS / ELECTRONIC MEMORY BUSINESS CONTEXT

- Two major implementations
  - Integrated memory for mid-range and high end central processing unit (CPU) products
  - Separable Memory (SIMMs) for workstation, personal computer (PC) and low end CPU products
- Physical architecture approaches
  - Packaging / design focused on lowest cost product at given functionality
  - Industry standard (highest volume, lowest cost) packaging
    + Integrated memory: small outline J bend (SOJ)
    + Separable memory: thin small outline package (TSOP)
- Product development cycle tied to CPU development cycle

2.4 UNIX SYSTEMS AND SOFTWARE (USS) CONTEXT

- **Platform strategy under development (workstations / servers)**
  - Alpha AXP workstations
  - VAX workstations
  - MIPS™ / UNIX ™workstations
  - RISC Servers
- **Physical architecture is primarily conventional with a mother board-daughter card approach for platform longevity**
- **18-month new product introduction cycles with a 9-month product enhancement cycle (mid-life kicker)**
- **Significant focus on competitiveness in commodity market.**

2.5 NETWORKS AND COMMUNICATIONS (NAC) CONTEXT

- Moving from "box products" to platforms
- Moving from follower of VLSI and packaging technology to parity
- Relatively long but decreasing product life cycles; full range of product volumes
- Corporate leader in electro-optics requirements

2.6 STORAGE PRODUCT CONTEXT

- **Product classes:**
  - Subsystems/controllers
  - Drives (tape/optical/disk)
- **Product features:**
  - Open: industry standard interfaces, standard form factors
  - Strong OEM focus
  - Competitive: cost and reliability driven
  - Short life cycles, high volumes
  - Families: common designs by size
- **Subsystems:**
  - Backplane-based platform strategy
- **Drives:**
  - Constrained to standard sizes, power, and capacity
  - Small form factor modules (down to 5 $inch^2$); very low height
  - Complex mixed signal technology (power, analog, digital; 20 - 200 MHz signals)
  - Power per chip < 1 watt
  - Less than 220 pins/chip
  - High density surface mount
  - Cabled (later - direct plugged)

2.7 PERSONAL COMPUTER SYSTEMS AND PERIPHERALS (PCSP) CONTEXT

- Move to product family and to platform approach.
  - Industry standard, Intel386 and Intel486 (deskside/desktop/laptop/notebook)
  - Printers
  - Video Terminals
- Move to greater use of industry "commodity" parts.
- Physical architecture approach is essentially SCP and mother board/daughter card - backplane. Very high integration and no backplane in video products for cost reduction.
- Varying product cycles; low to very high product volumes.
- Cost, reliability, time-to-market, small size and low power dissipation are major factors for PCSP.
- 9 months - 1 year development and product cycles.
- Compete in a commodity type market with industry - standard components.
- PC industry standard PWBs and connectors.

3 TECHNOLOGY STRATEGIES

The following subheads detail technology strategies.

3.1 CHIP TERMINATION STRATEGY

- Stitch wire bond (SWB) is the technology of choice for signal lead bonds through CMOS5
  - — SWB3: CMOS3, 150 micron pitch
  - — SWB4: CMOS4, 480 pads, 125 micron pitch
  - — SWB5: CMOS5, 600 pads, 112 micron pitch
- For CMOS6, assumption is that change from SWB is required (electrical performance) - CTT6
- Timing per technology roadmap

3.2 VLSI SINGLE CHIP PACKAGING

- Internal packaging and externally-sourced packaging must be consistent.
- The highest performance (flagship) packages will be pin grid arrays (100 mil standard; 100 x 50 mil optional).
- Surface mount (peripheral leaded) package development and use will be driven by the industry, not Digital, and industry standard packages will be used for most chips.
- We will be active in the development of industry standards.
- VLSI packaging must be fully consistent with modules strategy.
- We will minimize package variants.

3.2.1 SCP3

- Grid Array Packages
  - – Ceramic through-hole pin grid array (THPGA) (maximum 339 pins)
- Peripheral Leaded Packages
  - – Cerquad (maximum 164 pins)
  - – Leaded ceramic chip carrier (LDCC) (maximum 224 pins); use discouraged except when required
  - – Joint Electron Devic Engineering Council (JEDEC) plastic packages to 84 pins

3.2.2 SCP4

- Grid Array Packages
  - – Custom THPGA for NVAX (339 pins), EV4 (431 pins), R4000 (447 pins); external heat spreader, separable product-specific heat sink
  - – "Standard" grid arrays
  - – 100 x 50 THPGA is optional

- Peripheral Leaded Packages
  - PQFPs to 232 pins at 0.65mm
  - PQFPs to 240 pins at 0.5mm with restrictions:
    + Side 1 mounting only
    + Maximum PWB size: Eurocard
  - EIAJ Cerquad extension to 232 pins at 0.65mm or 240 pins at 0.5mm. 0.5mm has same restrictions as PQFP. Permanent heatsink is acceptable.

3.2.3 SCP5

- Grid Array Packages: extension of SCP4
  - Intrusive heat spreaders
  - Maximum pincount ~503
- Peripheral Leaded Packages
  - PQFPs at 0.5mm (304 pins)
  - Sub - 0.5 mm currently exploratory
  - Pincounts, body sizes per industry standard
  - Performance enhanced PQFPs (E-PQFP) may become viable, power / frequency limits TBD
- Chip on board (COB) currently exploratory

3.3 SMT PACKAGE STANDARD SIZE TABLE (For Selected Higher IO Formats)

Style	Pincount	Pitch	Body Size
PLCC (JEDEC)	44	50 mil	0.685 inch
	68	50 mil	0.980 inch
	84	50 mil	1.180 inch
Cerquad (manufactured by Digital)	44	50 mil	0.567 inch
	68	50 mil	0.872 inch
	84	50 mil	1.060 inch
	132	25 mil	0.872 inch
	164*	25 mil	1.060 inch
PQFP (EIAJ)	120/128	0.8 mm	28 mm
	144/160	0.65 mm	28 mm
	100	0.5 mm	14 mm
	144	0.5 mm	28 mm
	208	0.5 mm	28 mm
	232	0.65 mm	40 mm
	240	0.5 mm	28 mm
	304	0.5 mm	40 mm

* Extensions beyond 164 pins will follow EIAJ outline standard.

3.4 MULTICHIP PACKAGING

- EPWG strategy covers only internal applications of MCP / MCM technology.
- Only MCP currently in Digital products is MCU1 (VAX 9000).
- Further exploratory development in MCM-L and MCM-C technologies (thick film or cofired ceramic) is explicitly NOT recommended.
- When external MCPs or MCM-D units are used, outlines and module interface should be JEDEC specified.
- Further development of MCM-D technology, beyond infrastructural improvement, is explicitly NOT recommended.

3.5 CONNECTOR STRATEGY

- Historically, Digital has followed general industry trends but has been a leader in implementation - with concomitant difficulties.
- Six generations of backplane / connector systems have been deployed:
  - Soldered through-hole card edge (Digital Green Block)
  - Pressed pin card edge
  - Surface pressure ZIF (BI™)
  - Two-piece pressed pin (100 x 100)
  - Flex circuit (Aquarius)
  - Two-piece miniaturized (2mm Fbus)
- We will use industry-standard connectors.
- We will participate in SETTING these standards.
- Preferred Parts List (PPL) / Design Guide will be used for general purpose connector selection.
- Reduce to a minimum the introduction of new backplane connector technologies for traditional CPU, memory, and bus applications.
  - Develop a PPL / Design Guide.
  - Support technology enhancement to meet industry standards and performance advancement requirements.
- Invest to understand, characterize, and cost future technologies for unique high performance system requirements.
- SMT connectors currently in exploratory development.

3.6 PRINTED-WIRING BOARD STRATEGY

Context:

- System interconnect and critical timing paths continue to migrate toward the semiconductor device at a rapid pace.
- Product form factors are driving increased density.
- Cost, quality, and time-to-market remain as significant issues.

Strategy:

- Migrate board technology from unique Digital requirements to "state-of-the-shelf" industry norms.
- Emphasis on reduced set of well-characterized technology choices that lead to the lowest total system cost.
- Goal is to qualify PWB processes rather than PWB product components.

3.7 PRINTED-WIRING BOARD (PWB) GENERATIONS

Technology Platform	T3/T4	T5	T6
PWB* (Module)	**PWB 4**	**PWB 5**	**PWB 6**
Preferred Material	FR4	FR4	TBD
Total Layers	10	12	TBD
Max Aspect Ratio	9:1	9:1	TBD
Min Feature (Line)	0.005	0.004	TBD
Min Feature (Spacing)	0.005	0.004	TBD

* State-of-the-shelf Boundary Conditions

3.7.1 PWB 3 (HISTORICAL)

- Printed-wiring board technology driven towards the leading edge by the introduction of surface mount technology.
- Gate array-based CPUs pushed PWB technology towards higher density and connectivity.
- Module assembly processes and rework pushed PWB material selection toward higher Tg materials.

3.8 PWB 4

- Product paradigm shift toward microprocessor-based strategy places less pressure on PWB interconnect delay requirements.
- Increasing integrated circuit pin counts somewhat mitigated by higher percent of pins allocated to reference.
- Cost pressures drive PWB options (surface finish, soldermask, materials) to converge towards high volume lower cost industry norms.
- Low cost, high density, thin, printed-wiring boards emerging as a requirement for low cost, small form factor, electronic products.

3.8.1 PWB 5

- Increasing integrated circuit package pins (PGAs @ 500+ pins and surface mount @ 240 pins on less than 0.5 mm pitch) will drive high density line routing towards 4 mil lines and spacings.
- Greater emphasis on PWB technology characterization to provide a data base for informed decisions and trade-offs.
- Chip on board technology (currently exploratory) could impact PWB surface finish requirements.

- Continued pressure for low cost, dense, thin, boards for small form factor electronic products.

3.9 MODULE ASSEMBLY TECHNOLOGY STRATEGY

- Through-hole technology will continue to be used while it remains cost and performance competitive. Through-hole elimination is not a goal.
- MP3 process is **fully available** now. Continued investment will focus on:
  - Process excellence
  - Process standardization
  - Process management
- MP4 process is **under development** (FY93 qualification). Additional capabilities will include:
  - Limited 0.5mm SMT
  - Interstitial and high leadcount PGAs
  - Via in pad layout
- MP5 process requirements are in the definition phase.

3.9.1 MP3

- Mixed surface mount and through-hole assembly process using solder-screening, pick-and-place, convection IR reflow, through-hole insertion, wave solder and aqueous clean
- SMT Components to 224 lead LDCC/164 Lead Cerquad
- 339 lead PGA
- Emerging standard for general purpose module assembly within the company
- Process capable of being optimized for cost and quality at each site while retaining transferability of product
- No technological risks if designers work to preferred guidelines
- Continue to invest in process excellence and management

3.9.2 MP4

- MP4 is primarily an extension to MP3
- SMT components capability extended to 232 leads at 0.65mm pitch; 0.5mm components to 240 leads with restriction to single-sided use and Eurocard PWB
- THPGA to 447 pins at 100 or 100 x 50 mil pin pitch
- Via in pad layout rules

3.9.3 MP5

- MP5 capabilities are currently being defined.
- Expected to include very high leadcount THPGAs and peripheral-leaded 0.5mm SMT devices.
- May include sub-0.5mm SMT devices.
- Expected to include microminiature passives (0603) and SMT connectors.
- May include COB capabilities for modules and sub-modules (daughter cards).

3.10 BACKPLANE TECHNOLOGY STRATEGY

(To be added with the next revision of this document.)

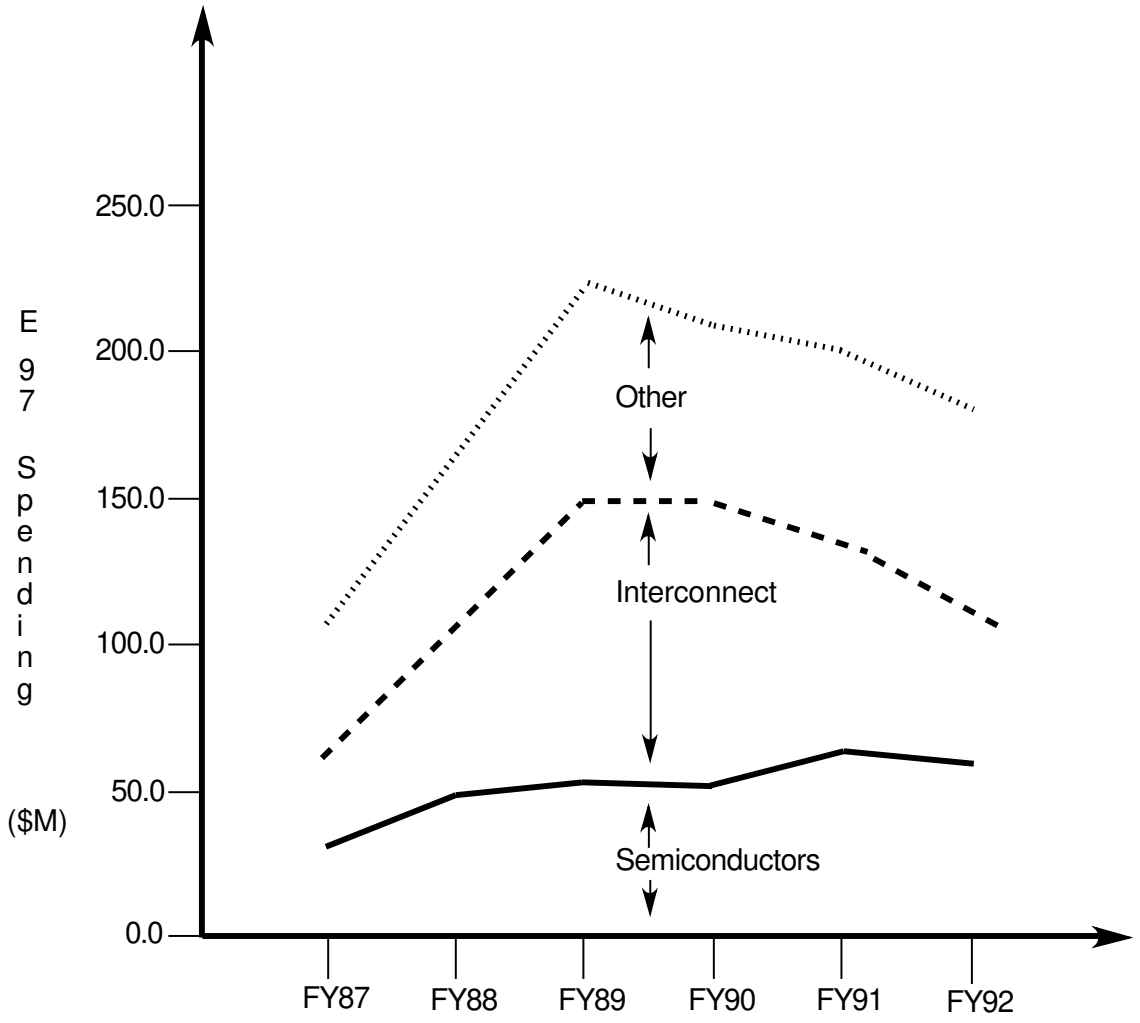
3.11 TECHNOLOGY RESEARCH AND ADVANCED DEVELOPMENT AGENDA

- It is vital to maintain our core competencies; AD at an appropriate level must be affirmed.
- Research in **defect prevention** will have a very significant payback.
- Chip packaging / powering / cooling will be the area of greatest apparent change (1000 pins, 1 GHz, 100w).
- New manufacturing techniques (for example, conductive adhesives, no-clean fluxes) are areas of interest.
- Electro-optics, cold electronics, and new packaging structures may be of long-term importance.
- We must be positioned to seize - and sometimes create - opportunities.
- Research portfolio is expected to include effective use of projects external to Digital.

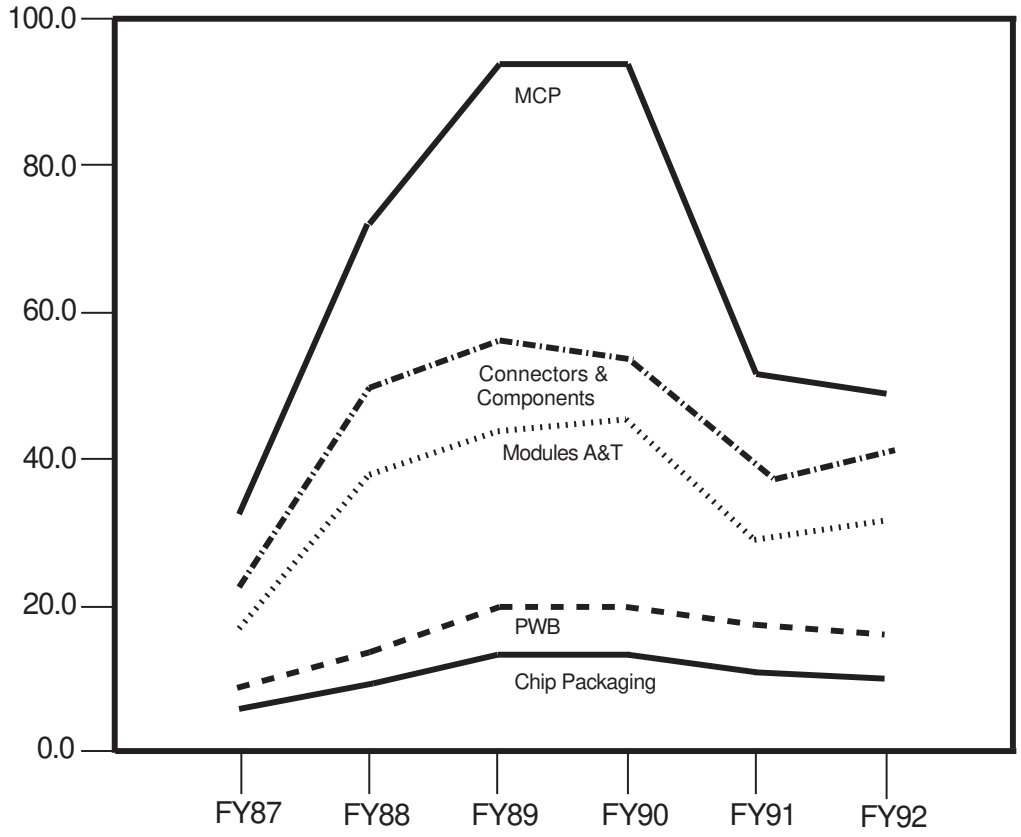
4 IMPLICATIONS

- **Adherence to the strategy will have major financial benefits.**
  - At least $50M / year savings in development
  - Associated downstream savings of at least $200M+ (operations)
- **Achieving the benefits of the strategy will require an unprecedented level of engineering / manufacturing discipline and communication.**
- **Funding allocations will be tied to the technology strategies.**
  - E97 will fund mainstream technology platforms.
  - Individual products will fully fund any development deviating from the strategy AND will continue to support a fair share of the mainstream.

4.1 ESTIMATED E97 SPENDING: FY87 - FY92 ($M)



4.2 ESTIMATED E97 INTERCONNECT SPENDING: FY87 - FY92 ($M)



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***FY92 numbers are Technology Task Force (TTF) Budget.**

5 TECHNOLOGY PLATFORM SPECIFICATIONS

The following subheads detail technology platform specifications.

5.1 CMOS TECHNOLOGY SPECIFICATIONS

		CMOS-3	CMOS-4	CMOS-5
Prototype year	FY89	FY91	FY93	FY96
Manufacturing year	FY90	FY92	FY94	FY97
CPU flagship	VAX 6000-300	VAX 6000-400	EV-5	EV-6
Vdd	3.3V	3.3V	3.3V	2.5V
Max chip size	1.4cm^2	2.0cm^2	3.0cm^2	4.0cm^2
Min feature	1.0µm	0.75µm	0.5µm	0.35µm
# levels metal	3	3	4	4
Average Transistors	0.8M	1.5M	4.0M	10M
Max Chip Pads	327	428	578	1000
Max Chip Power	10	15	60	100
µcycle period (ns)				
CISC	16	12	9	-
RISC	10	6.6	4.5	3

5.2 CHIP TERMINATION TECHNOLOGY SPECIFICATIONS

	SWB 3	SWB 4	SWB 5	CTT6
Prototype year	FY90	FY91	FY93	FY96
Manufacturing year	FY90	FY92	FY94	FY97
CPU flagship	VAX 6000-300	VAX 6000-400	EV-5	EV-6
Max pads	327	428	578	1000
Min pad pitch (μ)	150	125	112	TBD
Pad Configuration	Perimeter	Perimeter	Perimeter	Perimeter (2 row)
Interior pads	no	no	no	yes
Auxiliary capacitor	no	no	AD only	tbd
Max wire length (mils)	130	130	100-130	<15(bump)
Wire diameter (mils)	1.25	1.25	1.25	n/a
Wire material	Alum	Alum	Alum	n/a
Bond type	Wedge	Wedge	Wedge	Adhesive
Bond angle	45°	45°	30°	-
Barrier system	n/a	n/a	n/a	CTT-6
Passivation	oxide	oxide	oxide	TBD

5.3 VLSI SINGLE CHIP PACKAGING TECHNOLOGY SPECIFICATIONS

	SCP3	SCP4	SCP5	SCP6
Prototype Year	FY90	FY91	FY93	FY96
Manufacturing Year	FY90	FY92	FY94	FY97
Ceramic PGA				
Pins	339	447	503	1000
Power (w)	10	25	60	100
Max Frequency (MHz)	50	200	267	1000
Effective Pin Pitch (mils)	100	100/70	100/70	tbd
Custom MLC SMT				
Pins	224	↑	↑	↑
Power (w)	7			
Max Frequency (MHz)	50	n/a	n/a	n/a
Pin Pitch (mils)	25	↓	↓	↓
Cerquad SMT				
Pins	164	240		
Power	3.5	3.5	↑	↑
Max Frequency (MHz)	25	25		
Pin Pitch	25 mils	0.5mm	tbd	tbd
Construction	Cerquad	Cerquad	↓	↓
Outline	Custom SCO	EIAJ		
PLCC / PQFP				
Pins	84	232*	tbd	↑
Power	1	1.4	tbd	
Max Frequency (MHz)	25	25	tbd	tbd
Pin Pitch (min)	50 mil	0.65mm*	tbd	
Construction	PLCC	PQFP	PQFP	↓
Outline	JEDEC	EIAJ	EIAJ	

* 240 pins at 0.5mm allowed with restrictions. See SCP4 Strategy.

5.4 CONNECTOR TECHNOLOGY SPECIFICATIONS

(To be added with the next revision of this document.)

5.5 PWB (MODULE) ROADMAP*

	PWB 3	PWB 4	**PWB 5
Prototype Year	FY85	FY89	FY94
Manufacturing Year	FY86	FY90	FY95
Max Circuit Size	14 in×18 in	14 in ×18 in	14 in×18 in
End Point Test Grid	0.100	0.025	<0.025
Component Pitch	25 mils	0.50mm	≤0.5mm
Max Board Thickness	0.062	0.093	0.093
Min Board Thickness***	0.052	0.052	tbd
Dielectric (Er) @100 MHz	4.1	4.1	4.1
Max Number of Layers (Total)	8	10	12
Max Number of Layers (Sig/Pad)	6	6	8
Min Finished Hole Size	0.020	0.010	0.010
Min Thru Hole Pad Size	0.040	0.025	0.025
Max Aspect Ratio	5:1	9:1	9:1
Min as Drawn Line Width	0.006	0.005	0.004
Min as Drawn Line Spacing	0.010	0.005	0.004

* "State-of-the-shelf" Boundary Conditions

** May need to show metric dimensions

*** Module Process Constraint

5.6 MODULE ASSEMBLY TECHNOLOGY SPECIFICATIONS

	MP2	MP3	MP4	MP5
Prototype Year	FY85	FY89	FY92*	FY94*
Manufacturing year	FY86	FY90	FY93*	FY95*
Double-sided assembly	Yes	Yes	Yes	Yes
Passives	1206	0805	0805	0603/0402
SMT @ 0.050	Yes	Yes	Yes	Yes
SMT @ 0.025/0.65mm	No	to 224	to 232	to 232
SMT @ 0.5mm	No	No	to 240**	to 304
SMT sub - 0.5 mm	No	No	No	tbd
SMT connectors	No	No	No	tbd
DIPS/Axials	Yes	Yes	Yes	Yes
SOJ/TSOP/VSOP	No	Yes	Yes	Yes
100 mil THPGA	to 223	to 339	to 431	to 431
100×50 THPGA	No	No	to 447	to 503
TH Connectors	yes	yes	Yes	Yes
Max/Min PWB thickness	0.093/0.053	0.093/0.053	0.093/0.053	0.093/tbd

* **Note:** Availability of capabilities in MP4 and MP5 will be phased throughout the T4 and T5 windows.

** With restrictions

5.7 BACKPLANE TECHNOLOGY SPECIFICATION

(To be added with the next revision of this document.)

EPWG STRATEGY GLOSSARY

ASIP: Applications Specific Integrated Circuits and Packaging (UCF)

BI: Backplane Interconnect

CACC: Close Attch Chip Capacitor

Cerquad : Lead Frame-based Ceramic Quad Package

CMOS: Complimentary Metal Oxide Semiconductor

COB : Chip-on-Board

CPU : Central Processing Unit

CQUAD: Ceramic Quad

CTT : Chip Termination Technology

DCSS : Data Center Systems & Services

DIP : Dual In-Line Package

ECL: Emitter Coupled Logic

EIAJ : Electronics Industry Association, Japan (Standards Body)

ELS: Entry Level Systems

E-PQFP: Enhanced-plastic quad flat pack

ESB : Entry Systems Business

EVMS: Extended Virtual Memory System

HDSC : High Density Signal Carrier

IC: Integrated Circuit

ILB : Inner Lead Bonding

IR: Infra-red

ISB : Information Systems Business

JEDEC : Joint Electron Device Engineering Council (Standards Body)

LDCC : Leaded Ceramic Chip Carrier

LES : Low End Systems

MCC : Microelectronics Computer Technology Corporation

MCM : Multichip Module

MCM-C : MCM with Ceramic Substrate

MCM-L : MCM with Laminated Substrate

MCP : Multichip Packaging

MCU : Multichip Unit

MDT : Manufacturing and Design Technology

MLC : Multilayer Ceramic

MM : Micro Module (MCP)

NaC : Networks and Communications

NVAX: New VAX

OEM : Original Equipment Manufacturer

OLB : Outer Lead Bonding

PCSP : Personal Computer Systems and Peripherals

P/I : Packaging/Interconnect

PGA : Pin Grid Array

PLCC : Plastic Leaded Chip Carrier (J Bend)

PPL : Preferred Parts List

PQFP : Plastic Quad Flat Pack

PWB : Printed-Wiring Boards

QFP : Quad Flat Pack

RISC: Reduced Instruction Set Computer

SCO : Semiconductor Operations

SCP : Single Chip Package

SIMG : Storage & Information Management Group

SMT : Surface Mount Technology

SMPGA : Surface Mount Pin Grid Array

SOJ : Small Outline J (Bend)

SPA : Separable Pad Array

SWB : Stitch Wire Bond

TAB : Tape Automated Bonding

THPGA : Through-hole Pin Grid Array

TSOP : Thin Small Outline Package

TTF : Technology Task Force

UCF : Digital/Cupertino, CA

USS : Unix Systems and Software

Vdd : Drain Voltage

VIPS : Video Imaging and Printing Systems

VLSI : Very Large Scale Integration

VSOP : Very Small Outline Package

VSS : VAX Systems & Servers

ZIF : Zero Insertion Force

APPENDIX A REFERENCED DOCUMENTS

A.1 Digital Documents, EL-Class

Document Number	Document Title
EL-00084-00	*DEC STD 084-0 Process and Technology Phase Review Procedure*

A.2 Ordering Information

Use VTX SMC to order copies of EL-class Digital documents from Standards and Methods Control. Send distribution questions to JOKUR::SMC or call DTN: 234-4423.

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